REMARKS

I. Introduction

In response to the Office Action dated December 10, 2008, Applicant has amended claims 5, 9 and 13 in order to overcome the § 112 rejections and to further clarify the present disclosure. Support for the amendments may be found, for example, in paragraphs [0072], [0075]-[0076], [0097] and [0099]-[0107] of the Specification. Claim 8 has been cancelled, without prejudice. In addition, new claims 18-25 have been added. Support for new claims 18-25 may be found, for example, in paragraphs [0081]-[0082] and [0106]-[0107] of the specification. No new matter has been added.

For the reasons set forth below, Applicant respectfully submits that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claims 5-6, 13 And 15 Under 35 U.S.C. § 102

Claim 5 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Paton et al. (USP No. 7,091,097); and claims 5-6 and 13-15 are rejected as being anticipated by Keys (US 2004/0235280). Applicant respectfully traverses these rejections for at least the following reasons.

With regard to the rejection of claim 5 over Paton, the instant application claims priority to JP 2004-103681, which has a filing date of March 31, 2004, and this priority document supports the subject matter set forth in the pending claims. As the effective filing date thereof predates the filing date of Paton, which is September 3, 2004, it is respectfully submitted that Paton does not constitute valid prior art to the instant application. A certified English translation of JP 2004-103681 is being filed concurrently with this Amendment in order to perfect the claim

of priority. In view of the foregoing, it is respectfully submitted that the rejection based on Paton must be withdrawn.

Turning to the rejections over Keys, amended independent claims 5 and 13 each recite a method for manufacturing a semiconductor device, comprising the steps of: forming an amorphous layer in a region from a surface of a semiconductor region to a first depth; restoring a crystal structure of the amorphous layer in a region from the first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth; after the heat treating, forming a first impurity layer of a second conductivity type which has a pn junction at a third depth that is shallower than the second depth by introducing ions into the amorphous layer extending from the surface of the semiconductor region to the second depth; and restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth *using solid phase epitaxy*.

Features of the present disclosure in claims 5 and 13 for a method for manufacturing a semiconductor device include the steps of forming an amorphous layer in a region from a surface of a semiconductor region of a first conductivity type to a first depth, shrinking the amorphous layer to a second depth by heat treatment and restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy.

In contrast to the present disclosure, Keys teaches a method in which the remaining amorphous region 202 melts preferentially in the laser annealing process. For example, paragraph [0032] of Keys teaches in Fig. 2C how upon a second annealing, the dopants are diffused during melt with the amorphous region 202…[t]he second annealing is done with *a*

laser annealing process [which] preferentially melts the remaining amorphous region 202 in the substrate due to its lower melting temperature as compared to crystalline region 204." As such, it is clear that Keys does not use solid phase epitaxy as a method of restoring the crystal structure.

Thus, at a minimum, Keys does not teach the step of claims 5 and 13 of performing the second heat treatment by solid phase epitaxy to restore the crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth.

Anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently in a prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986). At a minimum, for the reasons set forth above, Keys does not disclose restoring a crystal structure of the amorphous layer in a region from the surface of the semiconductor region to the second depth using solid phase epitaxy. Therefore, as it is apparent from the foregoing that Keys fails to anticipate amended claims 5 and 13 or any dependent claims thereon, Applicant respectfully requests that the § 102 rejection be withdrawn.

Moreover, as claim 9 discloses this feature as well, Applicant submits that Keys also does not anticipate claim 9.

III. The Rejection Of Claims 5-17 Under 35 U.S.C. § 103

Claims 6, 13 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Paton et al. (USP No. 7,091,097) in view of Keys (US 2004/0235280); claims 7, 9 and 11 as being unpatentable over Paton in view of Yu (USP No. 6,521,502); claim 8 as being unpatentable over Paton in view of Wu (USP No. 6,391,751); claims 10, 14 and 16 as being unpatentable over Paton in view of Keys and further in view of Yu; claim 17 as being

unpatentable over Paton in view of Keys and further in view of Wu; claims 8 and 17 as being unpatentable over Keys in view of Wu; claims 7, 9-11, 14 and 16 as being unpatentable over Keys in view of Yu; claim 12 as being unpatentable over Paton in view of Yu and further in view of Wu; and over Keys in view of Yu and further in view of Wu. Applicant respectfully traverses these rejections of the pending claims for at least the following reasons.

As indicated above, Paton is not valid prior art based upon the claim of priority in conjunction with the filing of the certified English translation of the priority document JP 2004-103681. As such, all rejections over Paton are invalid. Accordingly, the only remaining § 103 rejections that are not based in some part on Paton are of claims 7, 9-12, 14 and 16, all of which are claims dependent upon either claim 5, 9 or 13.

As indicated above, Keys does not anticipate claims 5, 9 and 13. Moreover, Yu and Wu do not remedy this deficiency.

Yu teaches a process of forming a deep amorphous region 25 by implanting ions such as Si or Ge into a monocrystalline silicon substrate 12, forming a shallower source/drain extension layer 40, 42 by ion-implanting non-neutral dopants into the amorphous region and using solid phase epitaxy involving rapid thermal annealing (RTA) at a low temperature (500-600 °C), followed by recrystallization of the entire deep amorphous layer 25 and activating the non-neutral dopants.

The amorphous region 202 of Keys, which remains from the surface of the substrate to the depth D20, contains the recrystallization inhibitor 206. Therefore, the amorphous region cannot be recrystallized by RTA of Yu which is conducted at a low temperature. This is explained in paragraph [0028] of Keys, which describes that the region including the

recrystallization inhibitors 206 remains in the amorphous state after heat treatment in a temperature range of 400-800 °C. For this reason, Keys performs the annealing by laser at a temperature of 1200-1400 °C. As such, it is clear that the technique of Yu cannot be applied to Keys, because Yu performs the annealing via RTA solid phase epitaxy at a temperature far below that necessary for the annealing step in Keys.

In addition, Wu neither discloses, nor is relied upon to disclose, this feature of claims 5, 9 and 13. As such, it is clear that the combination of Keys with Yu and Wu fails to disclose or suggest each of the steps recited by any one of claims 5, 9 and 13. Accordingly, Applicant respectfully submits that claims 5, 9 and 13 are patentable and allowable over Keys, Yu and Wu, taken alone or in combination with one another.

Furthermore, under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 5, 9 and 13 are patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

Moreover, as new claims 18-25 are dependent upon allowable independent claims, Applicant submits that new claims 18-25 are allowable over the cited prior art as well.

IV. Conclusion

Having fully responded to all matters raised in the Office Action, Applicant submits that all claims are in condition for allowance, an indication of which is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Reg No 53,308

for Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF/NDM:kap
Facsimile: 202.756.8087
Date: March 10, 2009

Please recognize our Customer No. 53080 as our correspondence address.